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The Digital Processing Unit design approach for SERENA instrument on board BepiColombo

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In the frame of the BepiColombo ESA Mission, SERENA is a suite of four sensors coordinated by a centralized digital processing unit, namely the System Control Unit (SCU). Such computational unit will be equipped with a Field Programmable Gate Array (FPGA) based processor, in this case a Gaisler Research Leon 3 FT (Fault Tolerant) derived processor, able to provide instrument operations control and perform loss-less data compression. The Leon 3 FT represents one of the top reference processor for a space DPU FPGA based design and its validity is not further discussed in this context. At the same time, Information Technology revolution has pushed tremendous investments and efforts for designing outstanding Digital Signal Processor (DSP) devices as far as computational resources, power consumption, embedded memory resources, I/F flexibility are concerned, and for which the performances are far beyond any custom made chipset assembly of discrete parts or FPGA customizations. This work describes the design solutions adopted for fully saving the high reliability / rad-tolerant profile required for the mission, basing the DPU on a high reliability FPGA solution with the add-on of a DSP based compressor which may be excluded and eventually operated only after passing deep health checking testing.